IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Application of:	Examiner: Marcus T. Riley
Richard D. Taylor, et al.	Art Unit: 2625
Application No.: 10/826,886	Confirmation No.: 1435
Filed: 04/15/2004	
For: A PROGRAMMABLE I/O INTERFACE	

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APPELLANTS' APPEAL BRIEF

TO THE HONORABLE COMMISSIONER FOR PATENTS:

This brief is in support of a Notice of Appeal to the Board of Patent Appeals and Interferences filed on November 16, 2010, appealing the decision of the Examiner in the Non-Final Office Action mailed August 19, 2010 (hereinafter "Non-Final Office Action"), in which the claims of the above-captioned application were rejected for the sixth time. Appellants respectfully request consideration of this Appeal by the Board of Patent Appeals and Interferences ("BPAI") for allowance of the present patent application.

I. REAL PARTY IN INTEREST

The real party in interest in the above-identified application is Marvell International Technology Ltd. by virtue of assignments recorded in the U.S. Patent Office:

on 08/12/2004, at reel no. 015029, frame no. 0646;

on 02/22/2006, at reel no. 017206, frame no. 0666;

on 02/24/2006, at reel no. 017207, frame no. 0882; and

on 10/18/2007, reel no. 02000, frame no. 0001.

II. RELATED APPEALS AND INTERFERENCES

Appellants' undersigned representative and the assignee identified above are not aware of any other appeals or interferences that would directly affect or be directly affected by, or have a bearing on the BPAI's decision in the subject appeal.

III. STATUS OF CLAIMS

Claims 1, 3 and 5-12 are pending.

Claim 1 stands rejected under 35 U.S.C. § 112 as being indefinite.

Claims 1, 3 and 5-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over US 5,381,538 ("Amini") in combination with US 5,696,917 ("Mills"), US 6,029,239 ("Brown") and US 6,112,275 ("Curry").

Appellants respectfully traverse and appeal the rejection of claims 1, 3 and 5-12.

IV. STATUS OF AMENDMENTS

No claim amendment has been filed after receiving the Non-Final Office Action of August 19, 2010.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claims 1, 3 and 5-12 are directed towards a programmable input/output (I/O) interface. Support for the claims can be found throughout the specification as originally filed.

Independent claim 1

Independent claim 1 is directed to a programmable interface comprising a register file having a plurality of registers, each register having a type; a run control register; a microcontroller configured to bidirectionally communicate with the register file and the run control register; a Code Store SRAM configured to bidirectionally communicate with the microcontroller; and executable code including one or more instructions; wherein the Code Store SRAM and the run control register are configured to bidirectionally communicate with a system processor that is external to the programmable interface; wherein the system processor is configured to load the executable code onto the Code Store SRAM and is further configured to signal the microcontroller, via the run control register, to begin execution of the one or more instructions included in the executable code; and wherein the plurality of registers includes (i) a general-purpose microcontroller register, (ii) a timer register, (iii) an external input/output (I/O) interface register, (iv) an internal I/O register, (v) a shared register, (vi) an interrupt register, and (vii) a first-in, first-out (FIFO) register configured to communicate with a direct memory access (DMA) controller.

Fig. 1 illustrates a peripheral 10, which includes a register file 18 having a plurality of registers, a run control register 16, a microcontroller 12 and a Code Store SRAM 14 (paragraph 0012). The microcontroller 12 bidirectionally communicates with the register file 18 and the run control register 16 (see Fig. 1 and lines 4-5 of original claim 1), and the Code Store SRAM 14 bidirectionally communicates with the microcontroller 12 (see Fig. 1 and line 6 of original claim 1). Furthermore, the Code

Store SRAM 14 and the run control register 16 bidirectionally communicate with a main processor 30 (see Fig. 1 and lines 8-9 of original claim 1).

The main processor 30 loads executable codes onto the Code Store SRAM 14 (paragraph 14, lines 1-3). After the main processor 30 has loaded the code, the main processor 30 signals the microcontroller 12, via the run control register 16, to begin execution of one or more instructions included in the executable code (paragraph 14, lines 4-5).

As illustrated in Fig. 1, the plurality of registers included in the register files includes (i) a general-purpose microcontroller register, (ii) a timer register, (iii) an external input/output (I/O) interface register, (iv) an internal I/O register, (v) a shared register, (vi) an interrupt register, and (vii) a first-in, first-out (FIFO) register configured to communicate with a direct memory access (DMA) controller (paragraph 0016).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Rejection under 35 U.S.C. § 112

Whether claim 1 is indefinite under 35 U.S.C. § 112.

2. Rejection under 35 U.S.C. § 103(a)

Whether claims 1, 3 and 5-12 are unpatentable over Amini in combination with Mills, Brown and Curry.

VII. ARGUMENTS

1. Rejection under 35 U.S.C. § 112: Whether claim 1 is indefinite under 35 U.S.C. § 112.

Claim 1 is directed towards a programmable interface that includes, among other features, *a register file having a plurality of registers, each register having a type*. In the Non-Final Office Action of August 19, 2010, the Examiner alleges that it is not understood what the recited *each register having a type* means. The Examiner states that, for the purpose of continued examination, the Examiner has interpreted *type* to mean any

type of register. Appellants agree with the interpretation of the Examiner and respectfully submit that a *type* of register may mean any type of register. Accordingly, Appellants respectfully request that the rejection under U.S.C. § 112 be withdrawn.

2. Rejection under 35 U.S.C. § 103(a): Whether claims 1, 3 and 5-12 are unpatentable over Amini in combination with Mills, Brown and Curry.

Amini fails to disclose various features of independent claim 1

Claim 1 is directed towards a programmable interface that includes, among other features,

> a microcontroller …;
> a Code Store SRAM configured to bidirectionally communicate with the microcontroller; …
> wherein the Code Store SRAM …[is] configured to bidirectionally communicate with a system processor that is external to the programmable interface…

As the recited microcontroller is included in the programmable interface, and as the recited system processor is external to the programmable interface, this implies that the recited microcontroller and the recited system processor are two different components. The recited configuration is also illustrated in Appellants' Fig. 1. Also, the recited Code Store SRAM communicates bidirectionally with the microcontroller and also with the system processor.

The Examiner alleges that Amini's SRAM 34, microprocessor 30 and processor portion 20 of Fig. 1 disclose the recited Code Store SRAM, the recited microcontroller and the recited system processor, respectively. Amini, in Fig. 1, illustrates that the processor portion 20 includes the microprocessor 30 (also see Amini, col. 2, line 55). That is, Amini's microprocessor 30 is a part of Amini's processor portion 20. As Amini's processor portion 20 includes microprocessor 30, it is physically impossible for Amini's microprocessor 30 to be included in a programmable interface, while Amini's

processor portion 20 is external to the programmable interface. Hence, it is physically impossible for Amini's microprocessor 30 and processor portion 20 to be equated to the recited microcontroller and the recited system processor, respectively. Accordingly, Appellants respectfully submit that Amini fails to disclose the above recited feature of claim 1.

Furthermore, claim 1 recites that the

> a microcontroller configured to bidirectionally communicate with … the run control register; …
> wherein the … the run control register …[is] configured to bidirectionally communicate with a system processor that is external to the programmable interface…

For at least the above discussed reasons, Amini fails to disclose a programmable interface comprising the microcontroller and a system processor that is external to the programmable interface. Accordingly, Amini does not disclose a run control register that bidirectionally communicates with a microcontroller and also with a system processor that is external to the programmable interface, as recited in claim 1.

Mills also fails to disclose various features of independent claim 1

Moreover, claim 1 recites

> … executable code including one or more instructions; …
> wherein the system processor is configured to load the executable code onto the Code Store SRAM and is further configured to signal the microcontroller, via the run control register, to begin execution of the one or more instructions included in the executable code…

The Examiner acknowledges that Amini fails to disclose these features, but alleges that Mills does so. Specifically, the Examiner alleges that Mills discloses that "…The program associated with the selected game will be loaded into SRAM 240 and programs executing from SRAM 240 can be accessed, and hence executed…" While this arguably discloses that programs are loaded into Mills' SRAM 240 and also that programs executing from SRAM 240 can be accessed, Appellants respectfully submit that Mills

does not disclose a "system processor configured to . . . signal the microcontroller, via the run control register, to begin execution of one or more instructions included in the executable code." (Emphasis added). Rather, Mills merely discloses loading programs into the SRAM 240, and accessing the program from the SRAM 240.

Brown and Curry also fail to disclose various features of independent claim 1

Although Brown and Curry allegedly disclose various types of registers, Brown and Curry fail to cure the above discussed deficiencies of Amini and Mills.

For at least these reasons, Appellants respectfully submit that claim 1 is allowable over Amini, Mills, Brown and Curry. Claims 3 and 5-12 depend on claim 1, either directly or indirectly, thereby incorporating all recitations of claim 1. Therefore, claims 3 and 5-12 are also allowable over Amini, Mills, Brown and Curry.

CONCLUSION

Appellants respectfully submit that all the appealed claims in this application are patentable and requests that the Board of Patent Appeals and Interferences direct allowance of the rejected claims. Payment to cover the appeal fee has been made by Deposit Account. We do not believe any other fees are needed. However, should any other fees be necessary, please charge our Deposit Account No. 500393. In addition, please credit any overages to the same account.

Respectfully submitted,

Schwabe, Williamson & Wyatt, P.C.

Dated: 01/14/2011

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VIII. CLAIMS APPENDIX

1. A programmable interface comprising:

a register file having a plurality of registers, each register having a type;

a run control register;

a microcontroller configured to bidirectionally communicate with the register file and the run control register;

a Code Store SRAM configured to bidirectionally communicate with the microcontroller; and

executable code including one or more instructions;

wherein the Code Store SRAM and the run control register are configured to bidirectionally communicate with a system processor that is external to the programmable interface; and

wherein the system processor is configured to load the executable code onto the Code Store SRAM and is further configured to signal the microcontroller, via the run control register, to begin execution of the one or more instructions included in the executable code; and

wherein the plurality of registers includes (i) a general-purpose microcontroller register, (ii) a timer register, (iii) an external input/output (I/O) interface register, (iv) an internal I/O register, (v) a shared register, (vi) an interrupt register, and (vii) a first-in, first-out (FIFO) register configured to communicate with a direct memory access (DMA) controller.

2. (Cancelled)

3. A programmable interface, as defined in claim 1, wherein the external I/O interface-register includes an edge detect logic.

4. (Cancelled)

5. A programmable interface, as defined in claim 1, wherein the executable code implements a laser printer mechanism communications interface and a vertical top-of-page synchronization interface.

6. A programmable interface, as defined in claim 1, wherein the executable code is selected from a group that includes serial interfaces, parallel interfaces, serial peripheral interface (SPI), Synchronous Serial Interface (SSI), MicroWire, Inter Integrated Circuit (I2C), control area network (CAN), UART, IEEE1284, LCD interface, front panel interface, and MODEM.

7. A programmable interface, as defined in claim 1, wherein the system processor is configured to bidirectionally communicate with the register file.

8. A programmable interface, as defined in claim 1, wherein the timer register is configured to (i) increment independently based on a selected system timebase, (ii) generate timing for protocols to be implemented, and (iii) detect protocol timeout errors.

9. A programmable interface, as defined in claim 1, wherein the shared register is accessed by both the system processor and the microcontroller, and wherein the shared register is configured to emulate a peripheral status, wherein an access priority grants write access to either the system processor or the microcontroller for accessing the to the shared register.

10. A programmable interface, as defined in claim 1, wherein the external I/O interface register is configured to (i) facilitate the microcontroller to observe and control actual external electrical signals associated with a protocol of communications of the

programmable interface, and (ii) facilitate implementation of a control state machine in the microcontroller.

11. A programmable interface, as defined in claim 1, wherein the internal I/O register is configured to (i) facilitate an I/O subsystem to communicate with internal dedicated function blocks of the programmable interface.

12. A programmable interface, as defined in claim 1, wherein the interrupt register is configured to (i) facilitate an I/O subsystem to provide interrupt-driven status to the system processor.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.